ABSTRACT OF THE DISCLOSURE

A system and method for transferring data from circuitry disposed in a lower frequency clock domain actuated by a first clock signal to circuitry disposed in a higher frequency clock domain actuated by a second clock signal, wherein the first and second clock signals are provided in a predetermined frequency ratio. A latch gated by the first clock signal is operable to generate latched data, which is provided to a first register disposed in the higher frequency clock domain. The first register, clocked by a modified clock signal that is synthesized by a logic circuit using the second clock signal and a plurality of intermediary clock signals derived from the second clock signal, is operable to generate registered data. A second register is operable to synchronize the registered data into a data output for subsequent use by the circuitry disposed in the higher clock frequency domain.